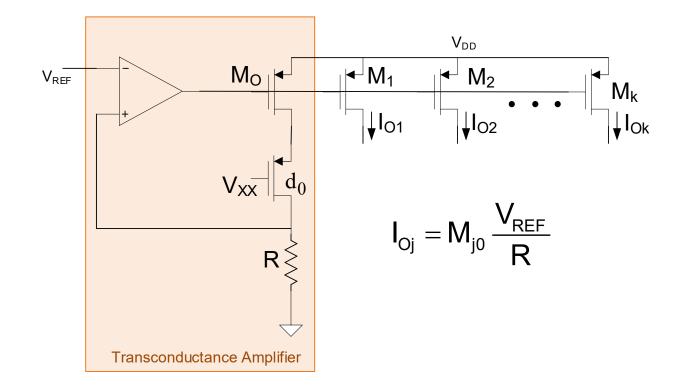
#### EE 435

#### Lecture 36

#### Charge Redistribution DACs ADC Design

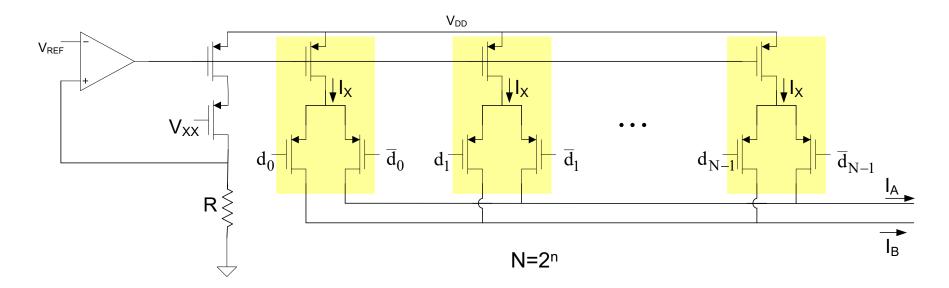
#### **Review from Last Lecture**

#### Multiple-output Transconductance Amplifier



- Good linearity
- Each additional output requires only one additional transistor

# Current Steering DAC with Supply Independent Biasing



If transistors on top row are all matched,  $I_X = V_{REF}/R$ 

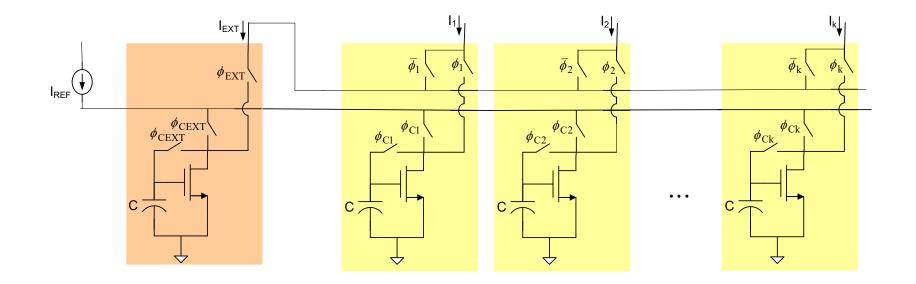
Thermometer coded structure (requires binary to thermometer decoder)

$$I_{A} = \left(\frac{V_{REF}}{R}\right)_{i=0}^{N-1} d_{i}$$

**Provides Differential Output Currents** 

**Review from Last Lecture** 

#### **Dynamic Current Source Matching**



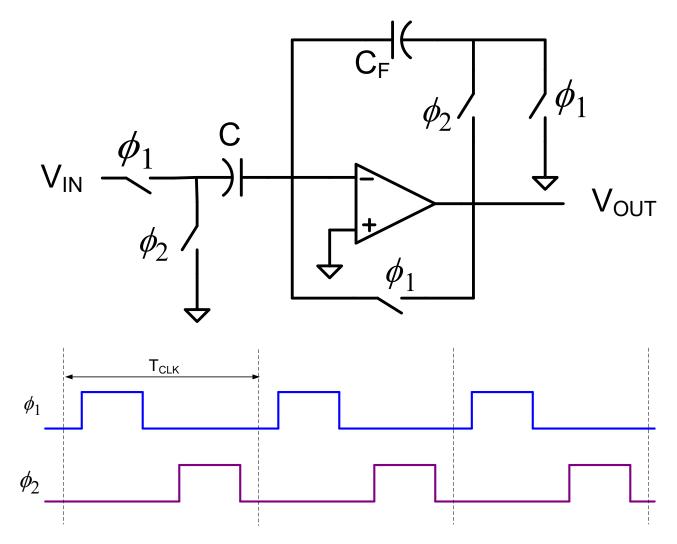
Extra current source can be added to facilitate background calibration

# Charge Redistribution DACs

- Previous DACs based upon matching of resistors or transistors
- Switch impedance was of concern in most of the structures
- Capacitor matching can be very good in most processes and area required for a given level of matching may be smaller for capacitors than for resistors or transistors in some processes
- Capacitor linearity is often excellent

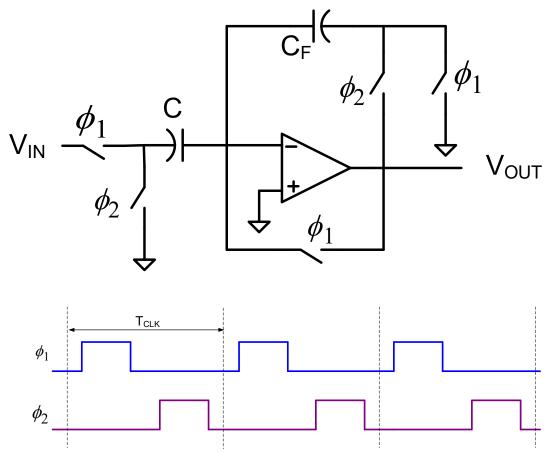
Will now focus on building DACs that take advantage of good capacitor matching and linearity

## A charge redistribution circuit



Clocks are complimentary non-overlapping

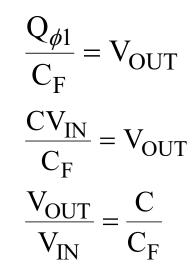
## A charge redistribution circuit



During phase  $\phi_1$ 

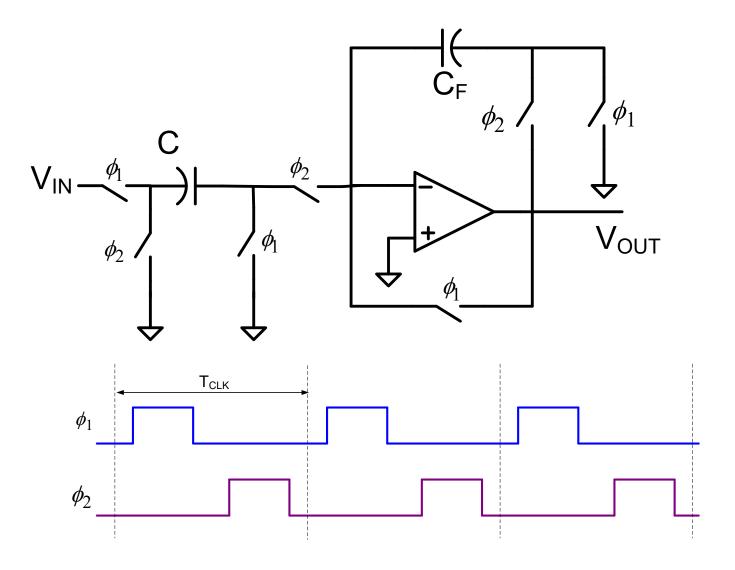
- $Q_{\phi 1} = CV_{IN}$  $Q_{CF} = 0$

During phase  $\varphi_2$ 

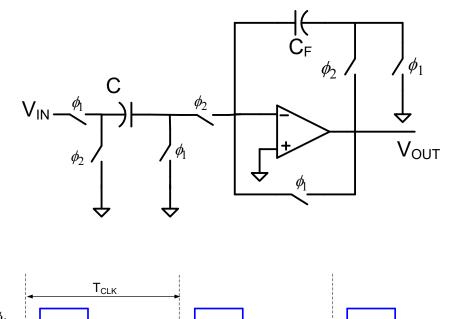


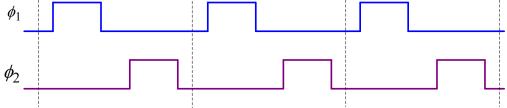
Serves as a noninverting amplifier Gain can be very accurate Output valid only during  $\Phi_2$ 

#### Another charge redistribution circuit



## A charge redistribution circuit



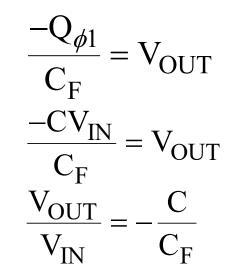


During phase  $\phi_1$ 

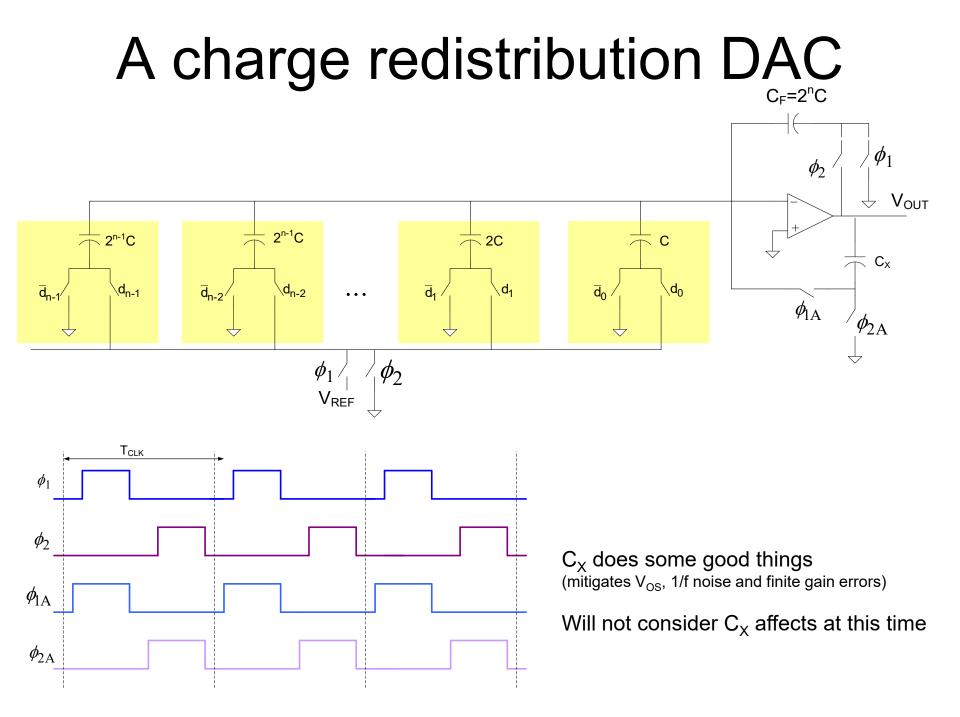
$$Q_{\phi 1} = CV_{IN}$$

 $Q_{CF} = 0$ 

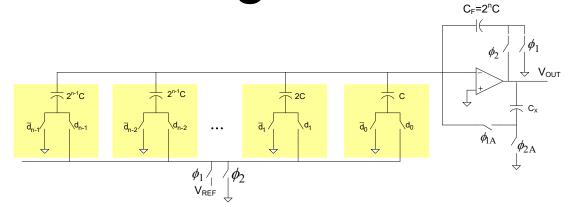
During phase  $\phi_2$ 



Serves as a inverting amplifier Gain can be very accurate Output valid only during  $\Phi_2$ 



### A charge redistribution DAC



During phase  $\phi_1$ 

$$\mathbf{Q}_{\phi 1} = \mathbf{V}_{\text{REF}} \sum_{i=0}^{n-1} \mathsf{d}_{i} \bullet 2^{i} \mathbf{C}$$

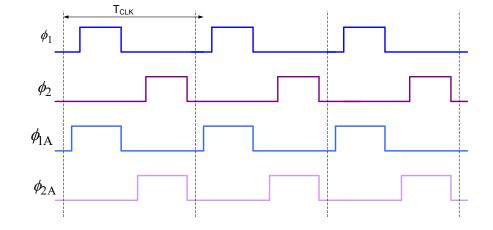
 $Q_{\rm CF} = 0$ 

During phase  $\phi_2$ 

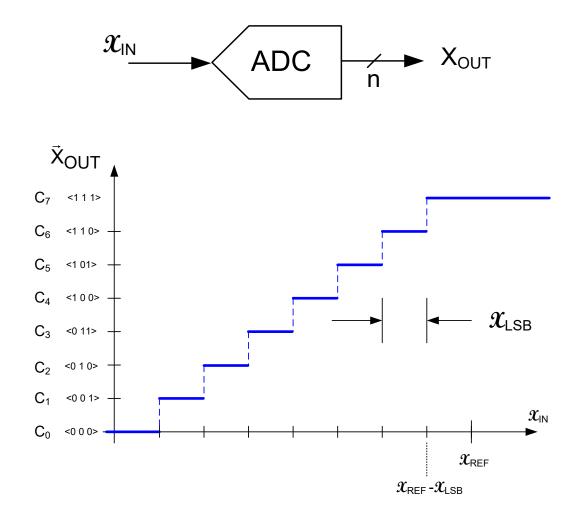
 $V_{OUT}(\phi_2) = \frac{1}{C_F} Q_{\phi 1}$ 

$$V_{OUT}(\phi_2) = \frac{1}{2^n C} V_{REF} \sum_{i=0}^{n-1} \mathsf{d}_i \bullet 2^i C$$

$$V_{OUT}(\phi_2) = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$



### Analog to Digital Converters



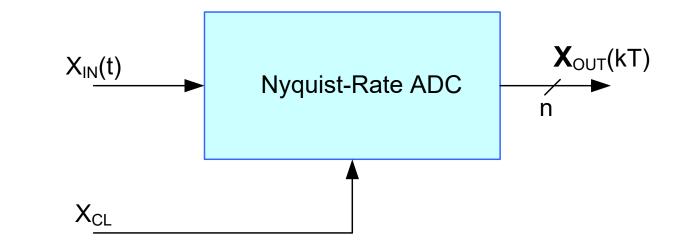
## Analog to Digital Converters

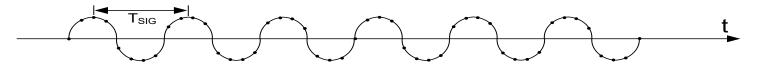
The conversion from analog to digital in most ADCs is done with comparators



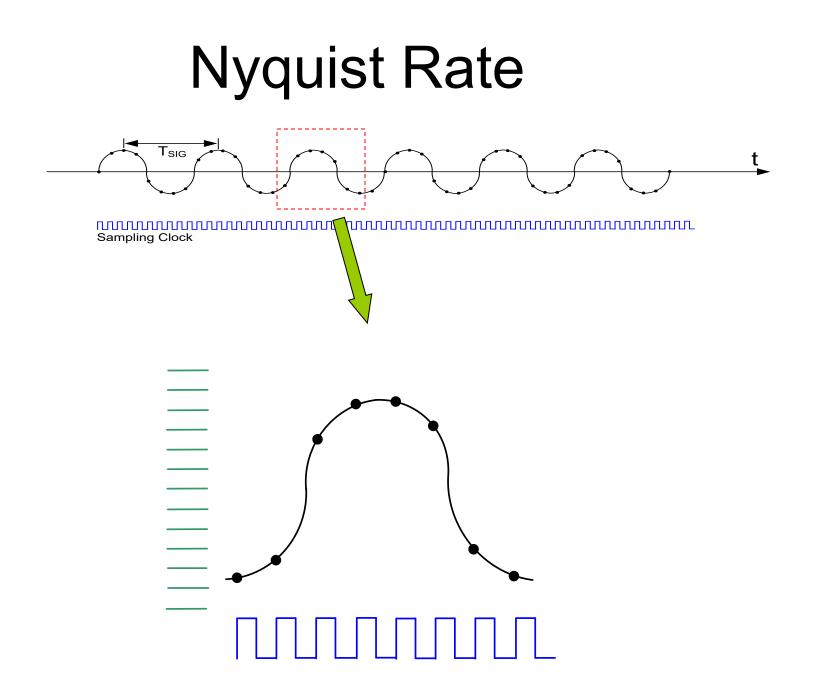
Most ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

### Nyquist Rate

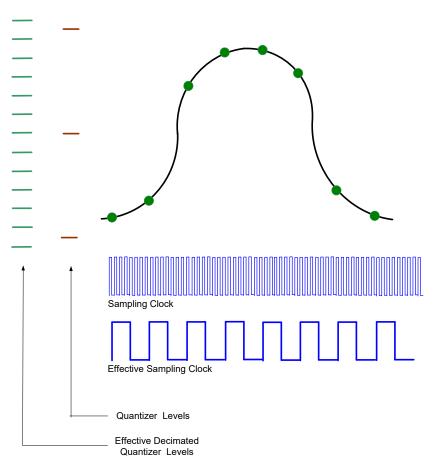




CONTRACTOR Sampling Clock

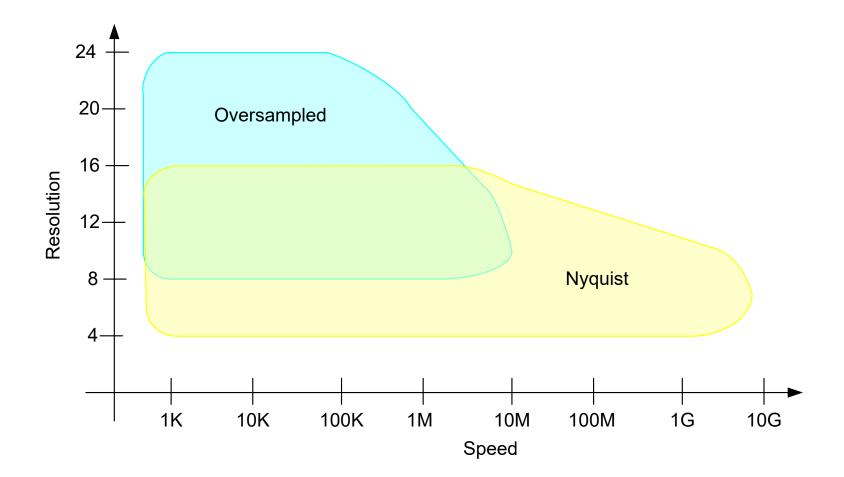


### **Over-Sampled**



Over-sampling ratios of 128:1 or 64:1 are common Dramatic reduction in quantization noise effects Limited to relatively low frequencies

### Data Converter Type Chart



# ADC Types

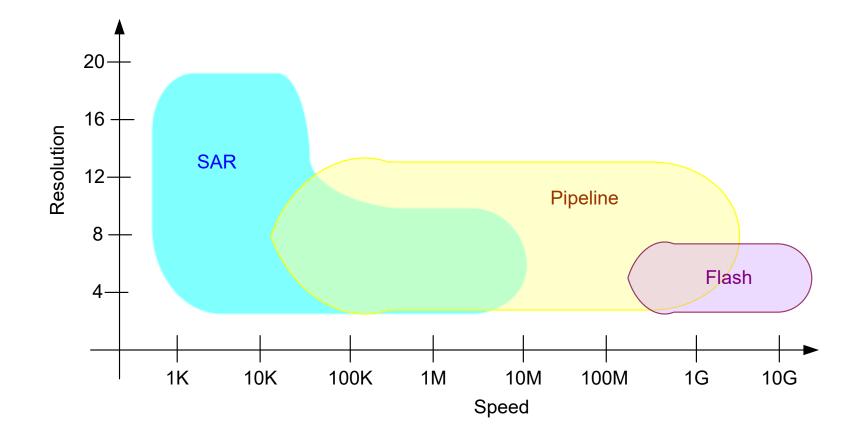
#### Nyquist Rate

#### **Over-Sampled**

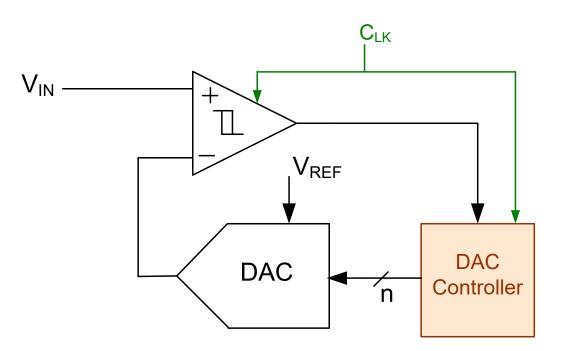
- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

## Nyqyist Rate Usage Structures



#### SAR ADC



- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small

# ADC Types

#### **Nyquist Rate**

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
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- Dual Slope

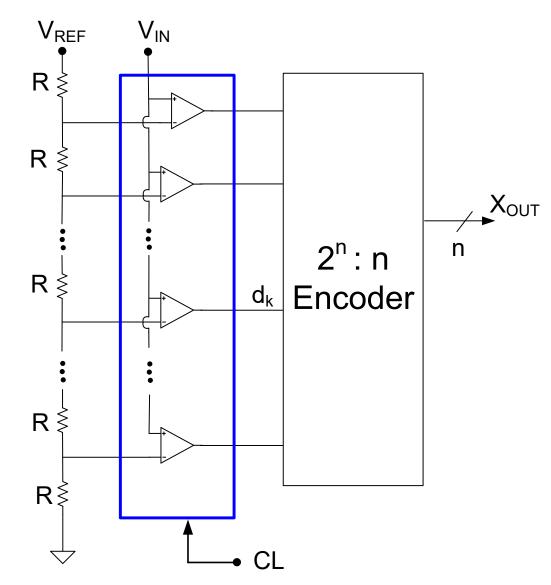
#### **Over-Sampled**

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

All have comparable conversion rates

Basic approach in all is very similar

#### Flash ADC





## Stay Safe and Stay Healthy !

#### End of Lecture 36